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- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negativeedge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the highto-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the  $\overline{Q}$ output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN7473, and the SN74LS73A are characterized for operation from 0 °C to 70 °C.

SN5473, SN54LS73A . . . J OR W PACKAGE SN7473 . . . N PACKAGE SN74LS73A . . . D OR N PACKAGE

#### (TOP VIEW)

	13 <b>]</b> 10
1K 🖾 3	12 10
Vcc□₄	
2CLK	10 <b>]] 2K</b>
	9 <sup>1</sup> 20
2J 🗗 7	8 20

73	
FUNCTION	TABLE

	INPUT	OUTPUTS				
CLR	CLK	J	К	٥	ā	
L	X	Х	X	L	н	
н	л	L	L	00	αo	
н	л	н	L	н	L	
н	л	L	н	L	н	
н	л	н	н	TOG	GLE	

'LS73A FUNCTION TABLE

INPUT	OUTP	UTS		
CLK	J	к	٩	ā
х	Х	Х	L	н
Ļ	L	L	ao	$\overline{\alpha}_{O}$
Ļ	н	L	н	L
1	L	н	L	н
1	н	н	TOG	GLE
н	x	x	ao	āo
	CLK X ↓ ↓	X X ↓ L ↓ H ↓ L ↓ H	CLK J K   X X X   ↓ L L   ↓ H L   ↓ H L   ↓ H H   ↓ H H	$\begin{array}{c ccccc} CLK & J & K & Q \\ \hline X & X & X & L \\ \downarrow & L & L & Q_{Q} \\ \downarrow & H & L & H \\ \downarrow & L & H & L \\ \downarrow & H & H & TOG \end{array}$

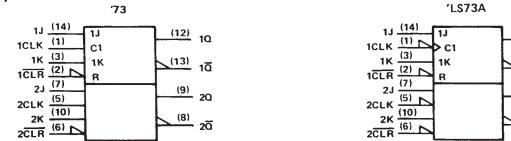
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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#### logic symbols<sup>†</sup>



(12) 10

<u>(13)</u> 10

20

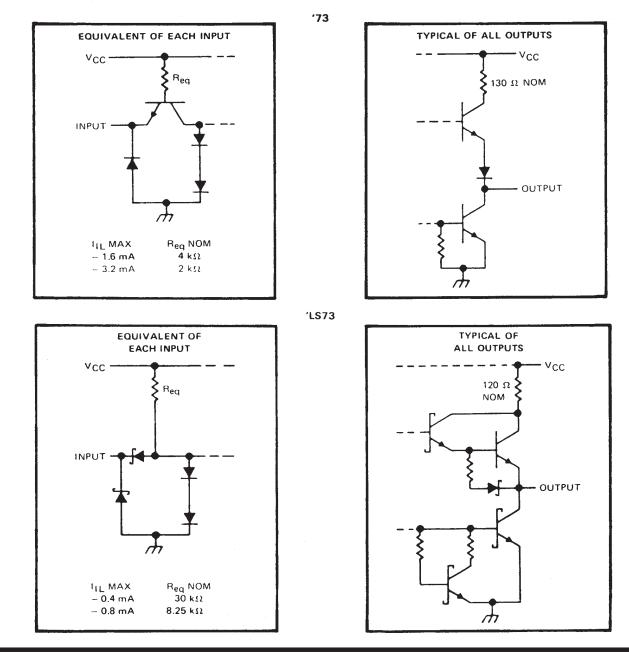
20

(9)

(8)

<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

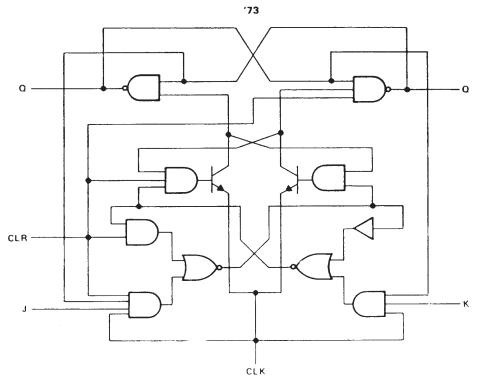
#### schematics of inputs and outputs



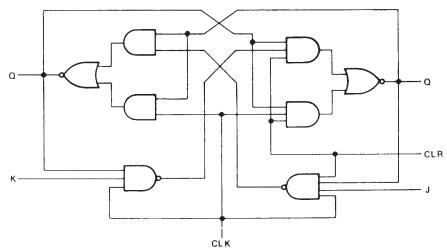


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### logic diagrams (positive logic)







## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, Vcc (See Note 1)	
Input voltage: '73	5.5 V
1S73A	7 V
	SN54' 55°C to 125°C
	SN74' 0° C to 70°C
Storage temperature range	

NOTE 1: Voltage values are with respect to network ground terminal.



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#### recommended operating conditions

			SN5473		SN7473				
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			_	0.8			0.8	V
ЮН	High-level output current				- 0.4			- 0.4	mA
IOL	Low-level output current	· · · · · · · · · · · · · · · · · · ·			16			16	mA
		CLK high	20			20	-		
tw	Pulse duration	CLK low	47			47			ns
		CLR low	25			25			
t <sub>su</sub>	Input setup time before CLK t		0			0			ns
th	Input hold time data after CLK↓		0		_	0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				int		SN5473		SN7473			UNIT
PARAMETER		TEST CONDITIONS <sup>†</sup>			MIN	TYP‡	MAX	MIN	TYP\$	MAX	
VIK		V <sub>CC</sub> = MIN,	l <sub>l</sub> = 12 mA				- 1.5			- 1.5	V
VOH		V <sub>CC</sub> = MIN, I <sub>OH</sub> = - 0.4 mA	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.8 V,	2.4	3.4		2.4	3.4		v
VOL		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16 mA	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> ≈ 0.8 V,		0.2	0.4		0.2	0.4	v
4		V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V				1			1	mA
Чн	J or K CLR or CLK	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 2.4 V				40 80			40 80	μA
	J or K						- 1.6			- 1.6	
1 <sub>1L</sub>	CLR	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V				- 3,2			- 3.2	] mA
	CLK		·				- 3.2			- 3.2	]
los§		V <sub>CC</sub> = MAX			- 20		- 57	- 18		- 57	mA
Icc1		V <sub>CC</sub> = MAX,	See Note 2			10	20	<u> </u>	10	20	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25 °C$ .

§ Not more than one output should be shorted at a time.

<sup>¶</sup> Average per flip-flop.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\overline{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

### switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$ (see note 3)

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	MAX	UNIT
f <sub>max</sub>				15	20		MHz
<sup>t</sup> PLH	CLR	ā.			16	25	ns
<sup>t</sup> PHL	CLN	٩	$R_{L} = 400 \Omega$ , $C_{L} = 15 pF$		25	40	ns
<sup>t</sup> PLH	CLK	$Q \text{ or } \overline{Q}$			16	25	ns
<sup>t</sup> PHL	ULK	2012			25	40	ns

#fmax = maximum clock frequency: tpLH = propagation delay time, low-to-high-level output; tpHL = propagation delay time, high-tolow-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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#### recommended operating conditions

			S	SN54LS73A		SN74LS73A			
			MIN NOM MAX MIN NOM		MAX	UNIT			
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	5.25	V.
VIH	High-level input voltage					2			V
VIL	Low-level input voltage				0.7			0.8	V
юн	High-level output current				- 0.4			- 0.4	mA
IOL	Low-level output current				4			8	mA
fclock	Clock frequency		0		30	0		30	MHz
•	Pulse duration	CLK high	20			20			
t <sub>w</sub>	Fulse duration	CLR low	25			20			ns
		data high or low	20			20			
t <sub>su</sub>	Set up time-before CLK4	CLR inactive	20			20			ns
t <sub>h</sub>	Hold time-data after CLK I		0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETED			et	SI	154LS7	BA	SI	UNIT		
PARAMETER		TEST CONDITIONS <sup>†</sup>		MIN	TYP#	MAX	MIN	TYP‡	MAX		
VIK		V <sub>CC</sub> = MIN,	t <sub>1</sub> = - 18 mA				- 1.5			- 1.5	V
v <sub>он</sub>		V <sub>CC</sub> = MIN, I <sub>OH</sub> = – 0.4 mA	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = MAX,	2.5	3.4		2.7	3.4		v
		$V_{CC} = MIN,$ $V_{IL} = MAX,$ $V_{IH} = 2V,$ $I_{OL} = 4 mA$			0.25	0.4		0.25	0.4	v	
VOL		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 8 mA	V <sub>IL</sub> = MAX,	V <sub>1H</sub> = 2 V,					0.35	0.5	v
	J or K						0.1			0.1	
4	CLR	V <sub>CC</sub> = MAX,	V1 = 7 V				0.3			0.3	mA
	CLK						0.4			0.4	
	J or K						20			20	
Чн	CLR	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 2.7 V				60			60	μA
	CLK						80			80	
	J or K						0.4			- 0,4	-
ΠL	CLR or CLK	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V				- 0.8			- 0.8	mA
los		V <sub>CC</sub> = MAX,	See Note 4		- 20		- 100	- 20		- 100	mA
ICC (T	otal)	V <sub>CC</sub> = MAX,	See Note 2		1	4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\overline{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded,

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

### switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	MAX	UNIT
f <sub>max</sub>				30	45		MHz
<sup>t</sup> PLH	CLR or CLK	Q or Q	$R_L = 2 k\Omega$ , $C_L = 15 pF$		15	20	ns
<sup>t</sup> PHL	CLH OF CLK	Q or Q	-		15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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9-Oct-2007

### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9675101QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9675101QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9675101QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9675101VCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9675101VCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9675101VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9675101VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN7473N	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN7473N	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN7473N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN7473N3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74LS73AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73AN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS73AN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS73ANE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS73ANE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54LS73AFD	OBSOLETE	LCCC	FK	20		TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS73AFD	OBSOLETE	LCCC	FK	20		TBD	POST-PLATE	N / A for Pkg Type

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins P	ackage Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SNJ54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS73AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS73AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD**: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



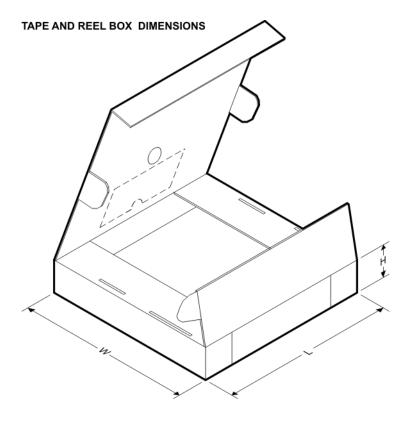
*All dimensions are nominal	
-----------------------------	--

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS73ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



# PACKAGE MATERIALS INFORMATION

11-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS73ADR	SOIC	D	14	2500	346.0	346.0	33.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MLCC006B - OCTOBER 1996

### FK (S-CQCC-N\*\*)

#### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



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		Wireless	www.ti.com/wireless